# LM64C142
## Passive Matrix Color LCD Unit

### FEATURES

- Display Format: 640 × 480
- Overall Dimensions:
  266.4 (W) × 182.3 (H) × 10 (D) mm
- Active Area: 192 (W) × 144 (H) mm
- Dot Pitch: 0.075 (W) × 0.275 (H) mm
- Response/Contrast Ratio: 300 ms/18:1
- Backlight: CCFT Single Edgelit

### DESCRIPTION

The SHARP LM64C142 Passive Matrix Color LCD unit is a 640 × 480 dots color display unit consisting of an LCD panel, a printed wiring board (PWB) with electric components mounted on it, tape automated bonding (TAB) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT backlight and bezel to fit them mechanically. Signal ground ($V_{SS}$) is connected with the metal bezel.

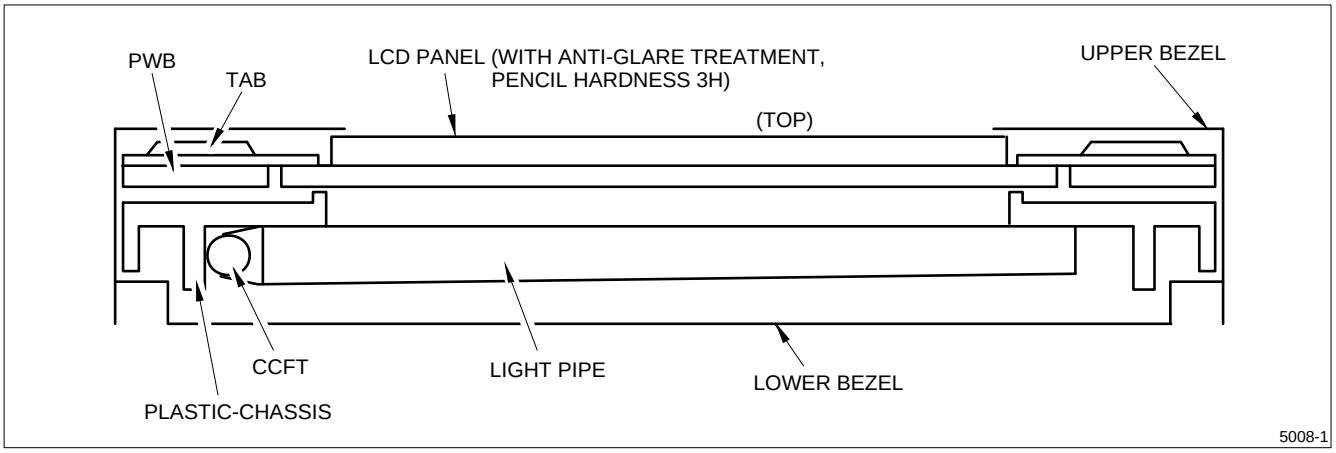
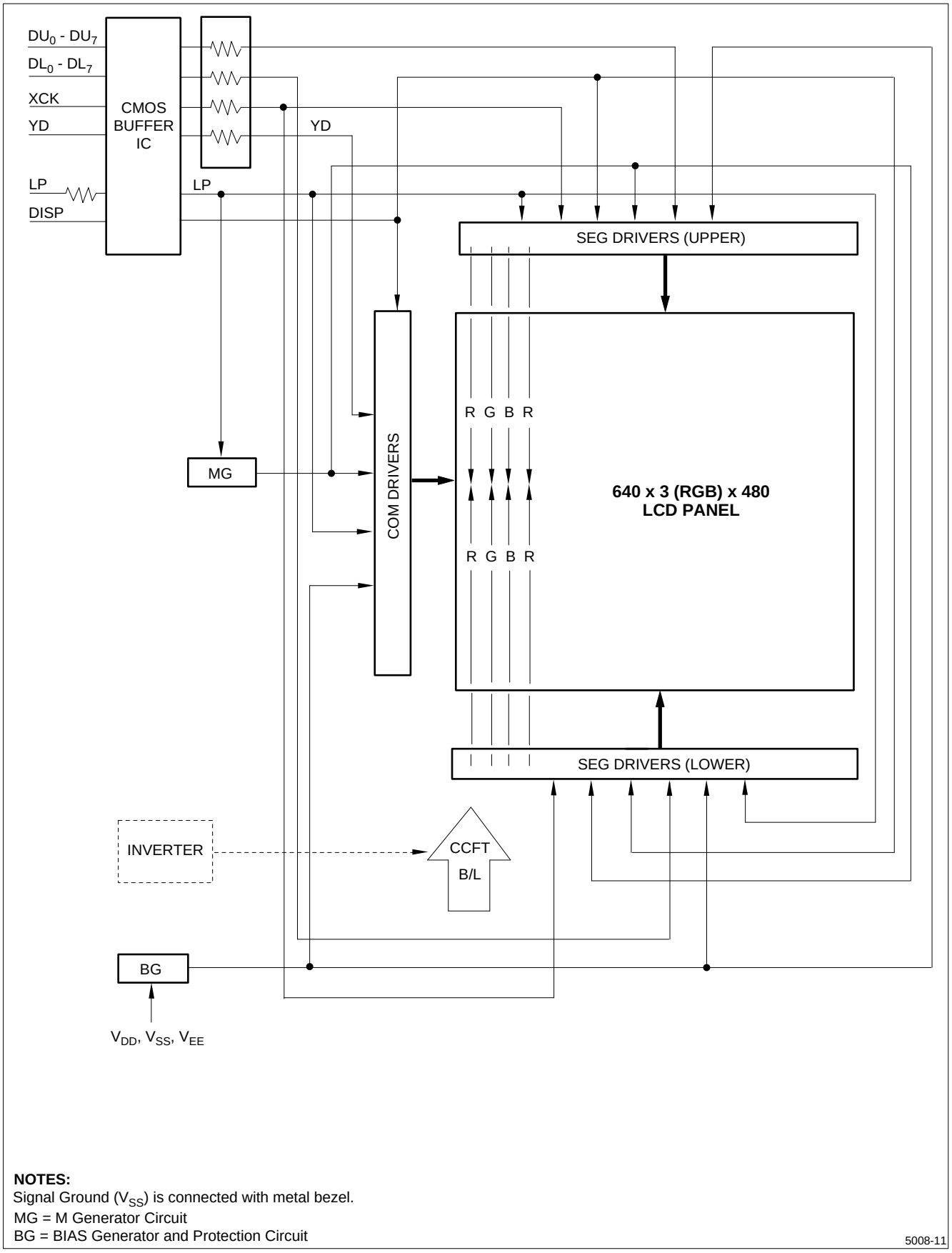



**Figure 1. LM64C142 Construction**




**LM64C142 Block Diagram**

## MECHANICAL SPECIFICATIONS

| PARAMETER | SPECIFICATIONS | UNIT | NOTE |
|---|---|---|---|
| Outline Dimensions | 266.4 (W) × 182.3 (H) × 10.0 max (D) | mm | – |
| Active Area | 191.975 (W) × 143.975 (H) | mm | – |
| Viewing Area | 195.0 (W) × 147.0 (H) | mm | – |
| Display Format | 640 (W) × 480 (H) Full Dots | – | – |
| Dot Size | 0.075 × RGB (W) × 0.275 (H) | mm | – |
| Dot Spacing | 0.025 | mm | – |
| Base Color | Normally Black | – | 1, 2 |
| Weight | Approximately 540 | g | – |

**NOTES:**

1. Due to the characteristics of the LC material, the colors vary with environmental temperature.
2. Negative-type display
   Display data 'H': Dots ON: Transmission
   Display data 'L': Dots OFF: Light isolation

## ABSOLUTE MAXIMUM RATINGS ($t_A$ = 25°C)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{DD} - V_{SS}$ | Supply Voltage (Logic) | 0 | 6.0 | V |
| $V_{EE} - V_{SS}$ | Supply Voltage (LCD drive) | 0 | 45.0 | V |
| $V_{IN}$ | Input Voltage | 0 | $V_{DD}$ | V |

## ENVIRONMENTAL CONDITIONS

| ITEM | TSTG | | TOPR | | CONDITION | NOTE |
|---|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | | |
| Ambient Temperature | –25°C | +60°C | 0°C | +40°C | Note 4 | 1 |
| Humidity | – | | – | | No condensation | 2 |
| Vibration | – | | – | | Three Directions (X/Y/Z) | 3 |
| Shock | – | | – | | Six Directions ( ±X ±Y ±Z) | 4 |

**NOTES:**

1. Do not subject the LCD Unit to temperatures out of this specification.
2. $t_A \leq 40$°C, 95% RH maximum.
   $t_A > 40$°C, Absolute humidity shall be less than $t_A = 40$°C/95% RH.
3. Two hours for each direction of X/Y/Z (six hours total).

| | | |
|---|---|---|
| Frequency | 10 Hz to 57 Hz | 57 Hz to 500 Hz |
| Vibration Level | – | 9.8 m/s$^2$ |
| Vibration Width | 0.075 mm | – |
| Interval | 10 Hz to 500 Hz to 10 Hz/11.0 min | |

4. Acceleration: 490 m/s$^2$
   Pulse width: 11 ms
   Three times for each direction of ±X ±Y ±Z.

## ELECTRICAL CHARACTERISTICS ($t_A$ = 25°C, $V_{DD}$ = 5 V ±5%)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|
| $V_{DD} – V_{SS}$ | Supply Voltage (Logic) | 4.75 | 5.0 | 5.25 | V | |
| $V_{EE} – V_{SS}$ | Supply Voltage (LCD Drive) | 23.0 | 26.9 | 32.6 | V | 1, 2 |
| $V_{IN}$ | Input Signal Voltage | 2.0 | – | $V_{DD}$ | V | 'H' Level, 5 |
| | | 0 | – | 0.8 | V | 'L' Level, 5 |
| $I_{IL}$ | Input Leakage Current | – | – | 1.0 | µA | 'H' Level |
| | | –1.0 | – | – | µA | 'L' Level |
| $I_{DD}$ | Supply Current (Logic) | – | 21.9 | 32.9 | mA | 3, 4 |
| $I_{EE}$ | Supply Current (LCD Drive) | – | 15.6 | 24.5 | mA | 3, 4 |
| $P_D$ | Power Consumption | – | 529.2 | 960.7 | mW | 3, 4 |

**NOTES:**

1. The viewing angle θ at which the optimum contrast is obtained by adjusting $V_{EE}$ - $V_{SS}$. Refer to Figure 6 for the definition of θ.
2. Maximum and minimum values are specified as the maximum and minimum voltage within the condition of the operational temperature range (0 - 40°C). Typical values are specified as the typical voltage at 25°C.
3. Display High Frequency Pattern:
   $V_{DD}$ = 5.0 V, $V_{EE}$ - $V_{SS}$ = 26.9 V, Frame frequency = 73 HZ
   Pattern Display = 4-bit checker.
4. This value is direct current.
5. TTL Level.

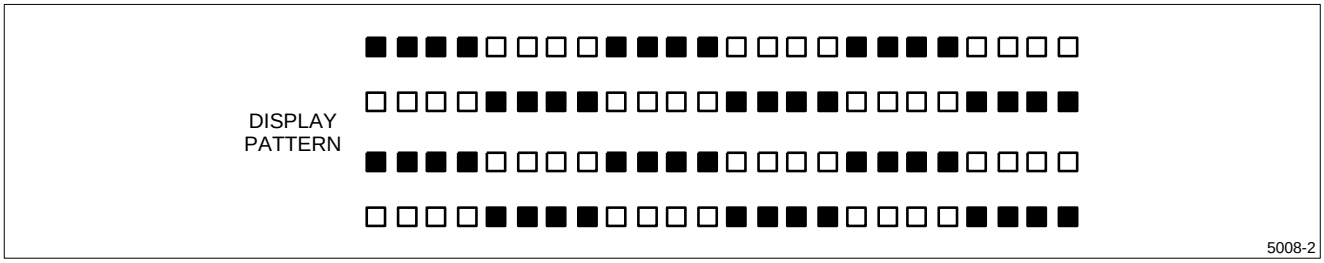



**Figure 2. Display High Frequency Pattern**

## INTERFACE SIGNALS

### LCD: CN1 [1]

| PIN NUMBER | SYMBOL | PARAMETER | LEVEL |
|---|---|---|---|
| 1 | YD | Scan Start-up Signal | H |
| 2 | LP | Input Data Latch Signal | H → L |
| 3 | XCK | Data Input Clock Signal | H → L |
| 4 | DISP | Display Control Signal | H (ON), L (OFF) |
| 5 | $V_{DD}$ | Power Supply For Logic and LCD (+5 V) | – |
| 6 | $V_{SS}$ | Ground Potential | – |
| 7 | $V_{EE}$ | Power Supply for LCD (+) | – |
| 8 | $DU_0$ | Display Data Signal (Upper) | H (ON), L (OFF) |
| 9 | $DU_1$ | | |
| 10 | $DU_2$ | | |
| 11 | $DU_3$ | | |
| 12 | $DU_4$ | | |
| 13 | $DU_5$ | | |
| 14 | $DU_6$ | | |
| 15 | $DU_7$ | | |

### LCD: CN2

| PIN NUMBER | SYMBOL | PARAMETER | LEVEL |
|---|---|---|---|
| 16 | $V_{SS}$ | Ground Potential | – |
| 17 | $DL_0$ | Display Data Signal (Lower) | H (ON), L (OFF) |
| 18 | $DL_1$ | | |
| 19 | $DL_2$ | | |
| 20 | $DL_3$ | | |
| 21 | $DL_4$ | | |
| 22 | $DL_5$ | | |
| 23 | $DL_6$ | | |
| 24 | $DL_7$ | | |
| 25 | $V_{SS}$ | Ground Potential | – |

**NOTES:**

1. Used connector: DF13A-15P-1.25H (21), DF13A-10P-1, 25H (21) (HIROSE).
   Mating connector: DF13-15S-1.25C, DF13-10S-1.25C (HIROSE).

### CCFT [1]

| PIN NUMBER | SYMBOL | PARAMETER | LEVEL |
|---|---|---|---|
| 1 | HV | High Voltage Line (From Inverter) | – |
| 2 | NC | – | – |
| 3 | GND | Ground Line (From Inverter) | – |

**NOTES:**

1. Used Connector: BHR-03VS-1 (JST)
   Mating Connector: SM03 (4.0) B-BHS or SM02 (8.0) B-BHS (JST)

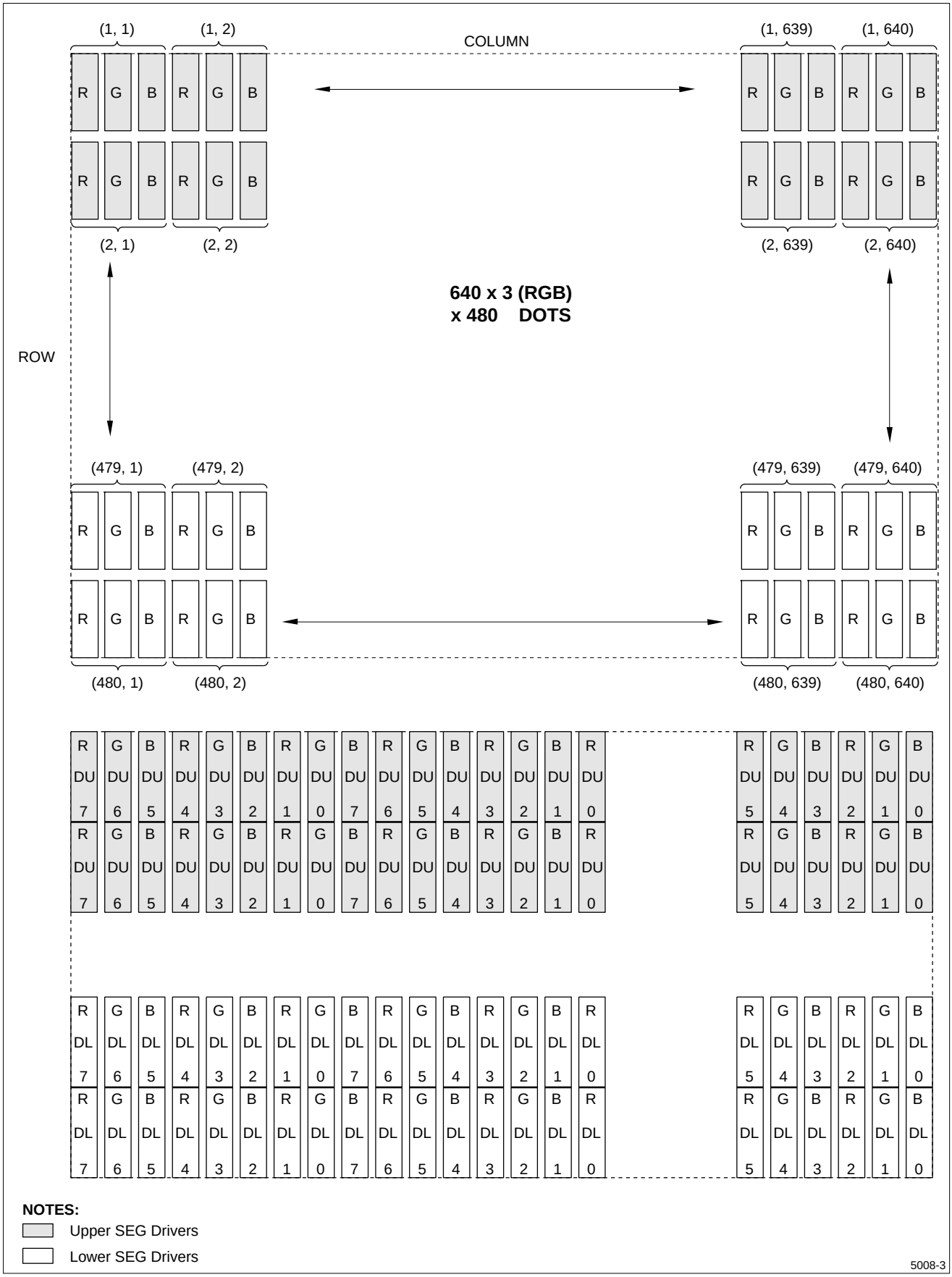



**Figure 3. Dot Chart of Display Area**

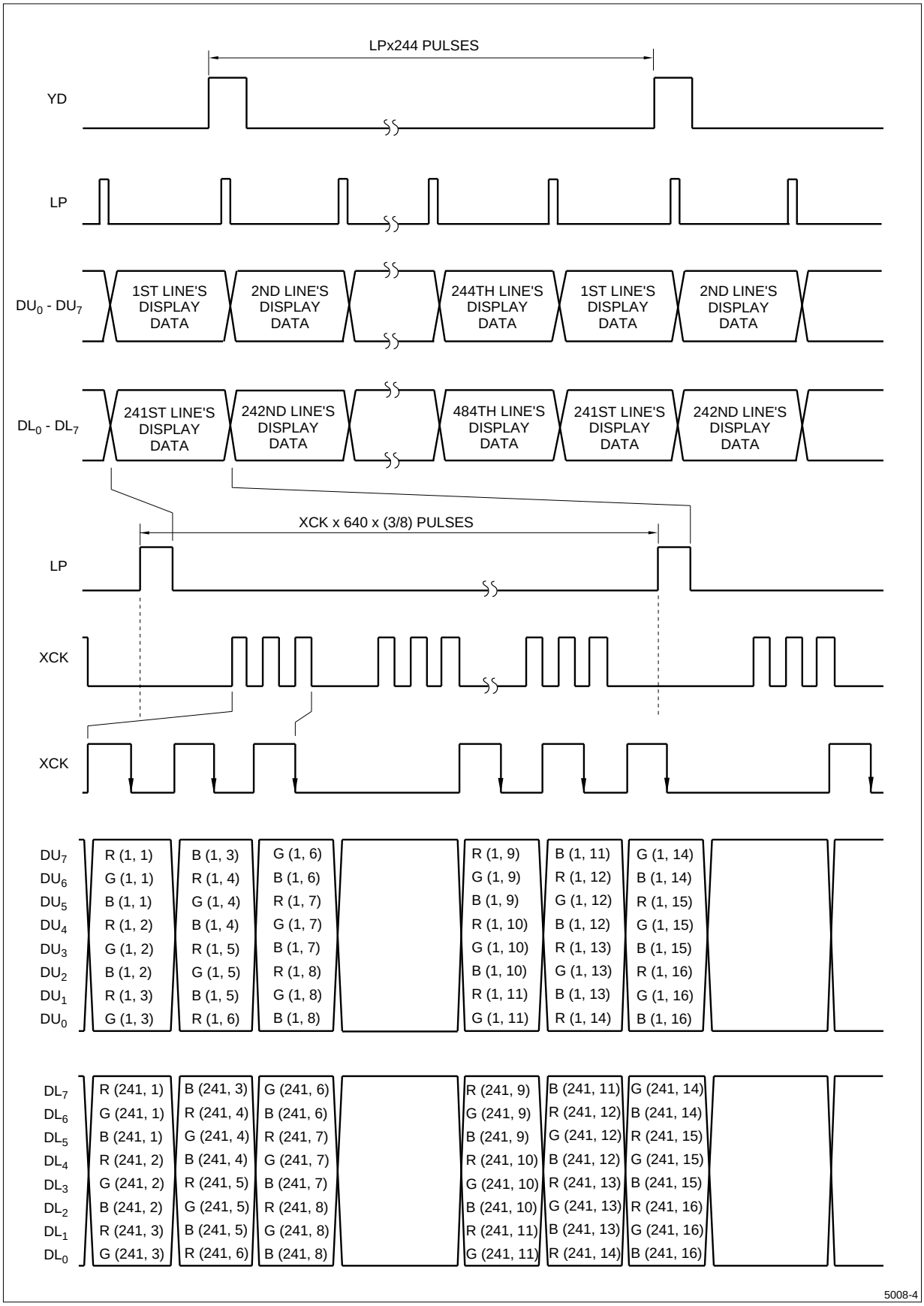



**Figure 4. Data Input Timing**

## INTERFACE TIMING RATINGS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS | NOTE |
|---|---|---|---|---|---|---|
| $t_{FRM}$ | Frame Cycle | 8.33 | – | 16.94 | ms | 1 |
| $t_{HYS}$ | YD Signal 'H' Level Set Up Time | 100 | – | – | ns | – |
| $t_{HYH}$ | YD Signal 'H' Level Hold Time | 100 | – | – | ns | – |
| $t_{LYS}$ | YD Signal 'L' Level Set Up Time | 100 | – | – | ns | – |
| $t_{LYH}$ | YD Signal 'L' Level Hold Time | 40 | – | – | ns | – |
| $t_{WLPH}$ | LP Signal 'H' Level Pulse Time | 200 | – | – | ns | – |
| $t_{CK}$ | XCK Signal Clock Cycle | 82 | – | – | ns | – |
| $t_{WCKH}$ | XCK Signal 'H' Level Clock Width | 30 | – | – | ns | – |
| $t_{WCKL}$ | XCK Signal 'L' Level Clock Width | 30 | – | – | ns | – |
| $t_{DS}$ | Data Set Up Time | 30 | – | – | ns | – |
| $t_{DH}$ | Data Hold Time | 30 | – | – | ns | – |
| $t_{LS}$ | LP ↑ Allowance Time From XCK ↓ | 200 | – | – | ns | – |
| $t_{LH}$ | XCK ↑ Allowance Time From LP ↓ | 200 | – | – | ns | – |
| $t_R$, $t_F$ | Input Signal Rise/Fall Time | – | – | 13 | ns | – |

**NOTE:**

1. LCD unit functions at the minimum frame cycle of 8.33 ms (Maximum frame frequency of 120 Hz). Due to the characteristics of LCD unit, 'shadowing' becomes more eminent as frame frequency goes up, while flicker is reduced. According to our experiments, frame cycle of 12.8 ms minimum or frame frequency of 78 Hz maximum demonstrates optimum display quality in terms of flicker and 'shadowing.' Since judgment of display quality is subjective and display quality such as 'shadowing' is pattern dependent, decide frame cycle or frame frequency, to which power consumption of the LCD unit is proportional, based on thorough testing on the LCD unit with every possible pattern displayed on it.

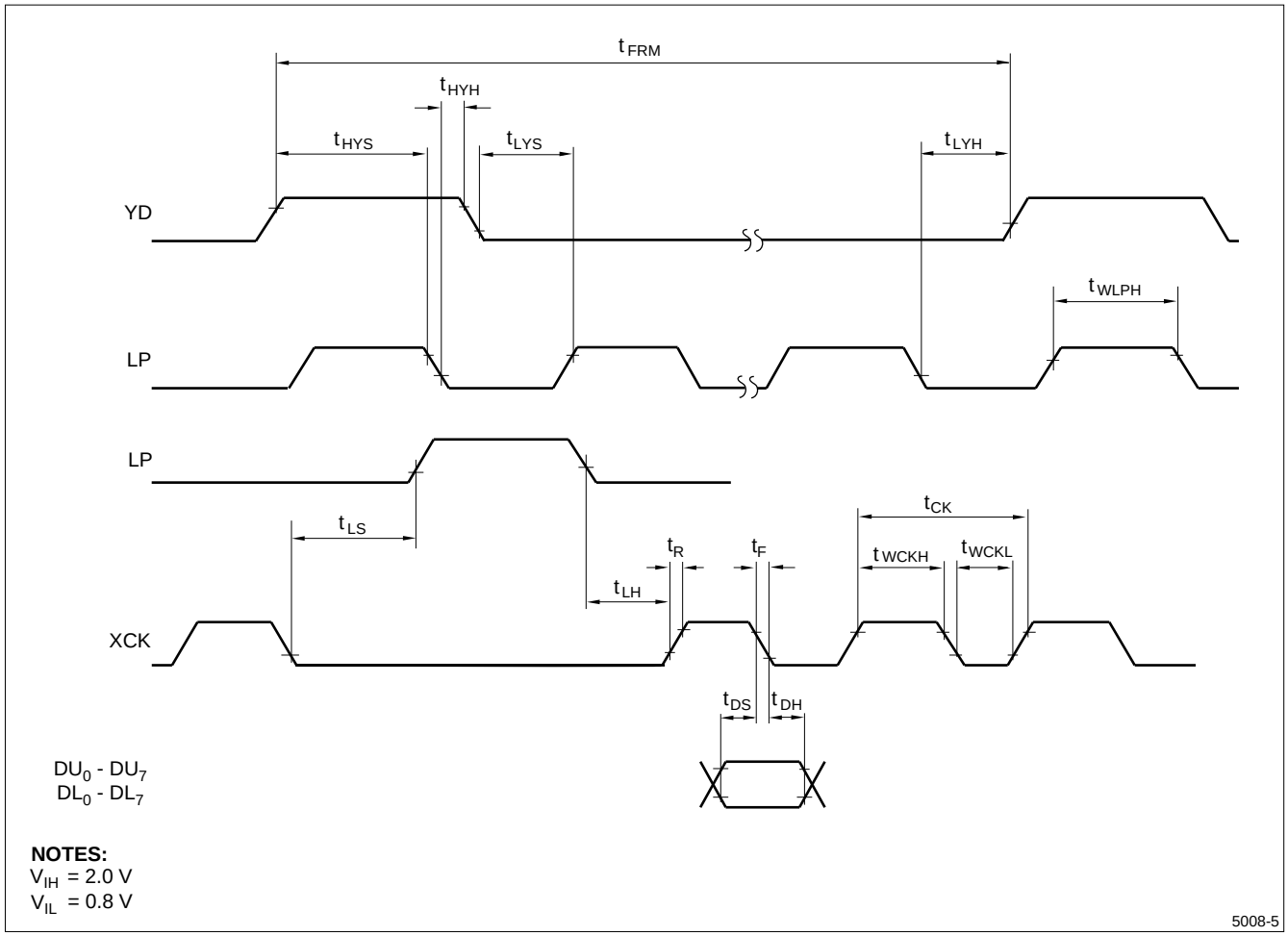



**Figure 5. Interface Timing Chart**

## UNIT DRIVING METHOD

### Circuit Driving Method

Figure 2 shows the block diagram of the unit's circuitry.

### Display Face Configuration

The display consists of 640 × 3 (RGB) × 480 dots. There is a single panel with single drive driven at 1/244 duty ratio.

### Input Data and Control Signal

The LCD driver is 160 bits LSI, consisting of shift registers, latch circuits, and LCD driver circuits. Input data for each row (640 × 3 RGB) are sequentially transferred in the form of 8-bit parallel data through shift registers from the top left of the display face together with the Clock Signal (XCK).

When input of one row (640 × 3 RGB dots) is completed, the data are latched in the form of parallel data corresponding to the signal electrodes by the falling edge of the Latch Signal (LP). Then the corresponding drive signals are transmitted to the 640 × 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) is transferred from the scan signal driver to the first row of scan electrodes, and the contents of the data signals are displayed on the first rows of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the first rows of data for 640 × 3 dots are being displayed, the second rows of data are entered. When 640 × 3 dots of data have been transferred, they are latched on the falling edge of LP, switching the display to the second row.

Such data input is repeated up to the 244th row of each display segment, from upper to lower rows, to complete one frame of display by time-sharing method.

Simultaneously, the same scanning sequence occurs at the lower panel. The input then proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which deteriorates the LCD panel, drive waveform is inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up with the clock frequency XCK. To minimize data transfer speed of XCK clock, the driver LSI applies the system of transferring 8-bits parallel data through the eight lines of shift registers. This system minimizes power consumption of the display unit.

In this circuit configuration, 8-bit display data is input pins of $DU_0 – DU_7$ and $DL_0 – DL_7$.

The LCD unit also adopts a bus line system for data input to minimize the power consumption. In this system, data input terminal of each driver LSI activates only when relevant data input is fed.

Data input for column electrodes of both upper and lower display segment and chip select of driver LSI are made as follows:

- The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 160 dots data (20 XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.
- This process is immediately followed at the column driver's LSIs of both the upper and the lower display segments. Thus, data input for both the upper and the lower display segments must be fed through 8-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no refresh RAM, it requires data and timing pulse inputs even for static display.

## OPTICAL CHARACTERISTICS ($t_A$ = 25°C, $V_{DD}$ = 5.0 V, $V_{EE}$ – $V_{SS}$ = $V_{MAX}$)

The following specifications are based on the electrical measuring conditions, on which the contrast of perpendicular direction (θx = θy = 0°) is maximum.

| SYMBOL | PARAMETER | CONDITION | | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|
| θx | Viewing Angle Range | $C_0$ > 5.0 | θy = 0° | –30 | – | 30 | degrees | 1 |
| θy | | | θx = 0° | –25 | – | 15 | | |
| $C_0$ | Contrast Ratio | θx = θy = 0° | | 10 | 18 | – | – | 2 |
| $t_R$ | Response Time – Rise | θx = θy = 0° | | – | 210 | 290 | ms | 3 |
| $t_D$ | Response Time – Decay | θx = θy = 0° | | – | 90 | 110 | ms | |
| x | Unit Chromaticity – White | θx = θy = 0° | | – | 0.277 | – | – | – |
| y | | θx = θy = 0° | | – | 0.329 | – | – | – |

**NOTES:**

1. The viewing angle is defined in Figure 6.
2. Contrast Ratio is defined as follows:

$$Co = \frac{\text{Luminance (brightness) all pixels 'white' at } V_{MAX}}{\text{Luminance (brightness) all pixels 'dark' at } V_{MAX}}$$

3. The response characteristics of the photodetector output are measured as shown in Figure 9, assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Figure 10.

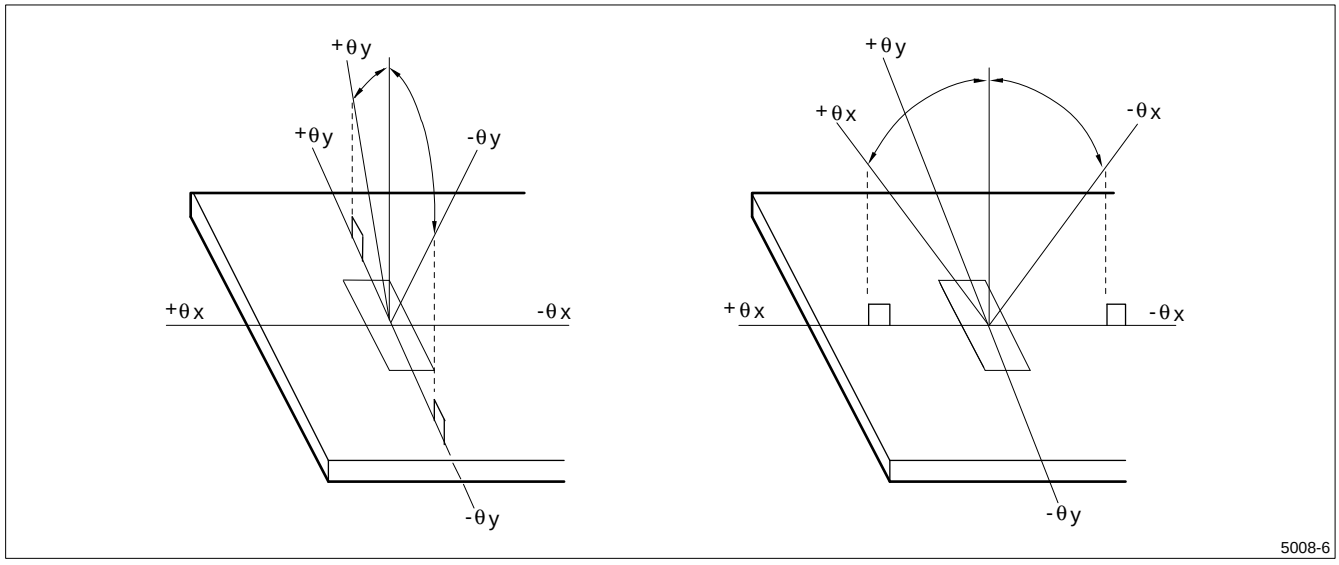



**Figure 6. Definition of Viewing Angle**

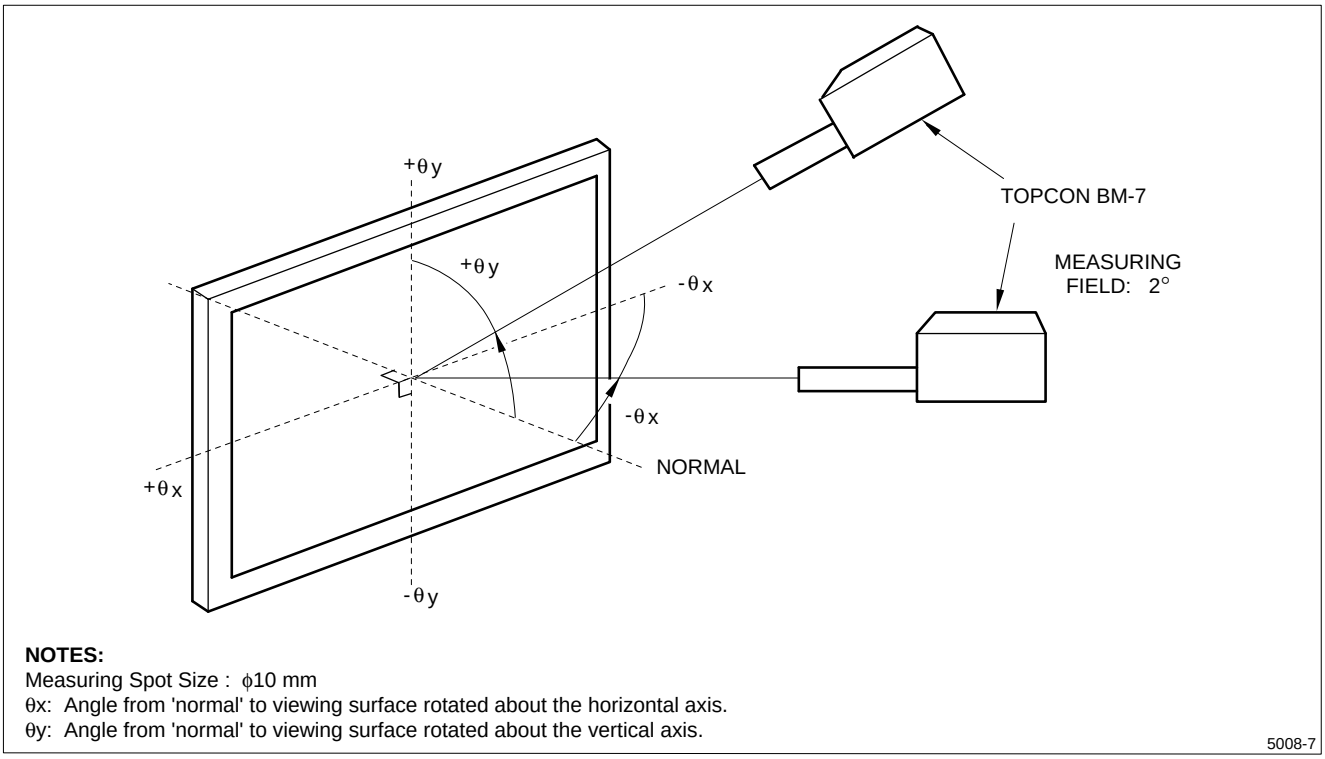



**Figure 7. Optical Characteristics Test Method I**

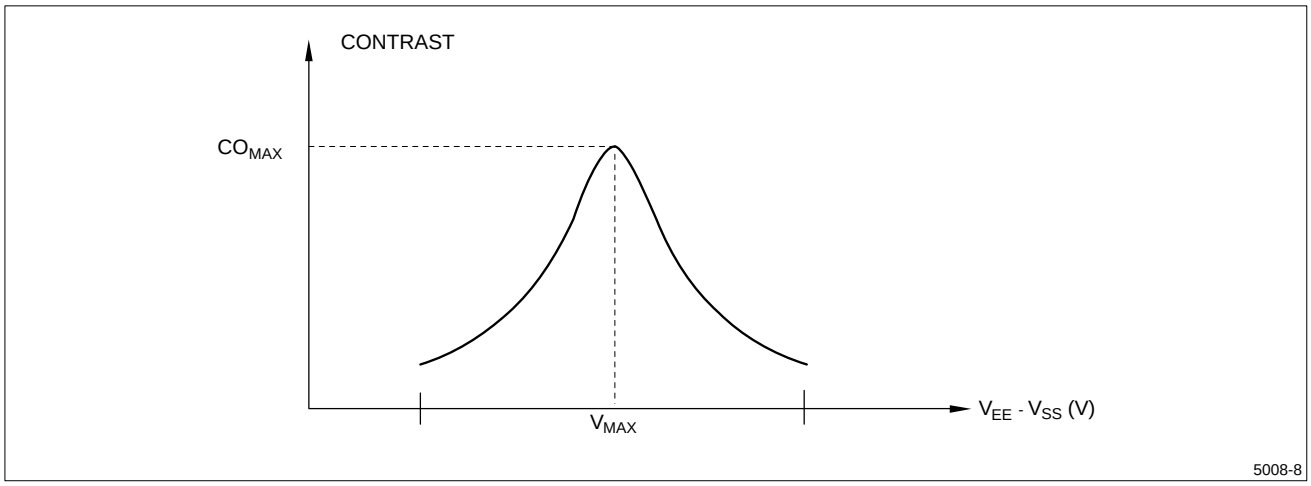



**Figure 8. Definition of $V_{MAX}$**

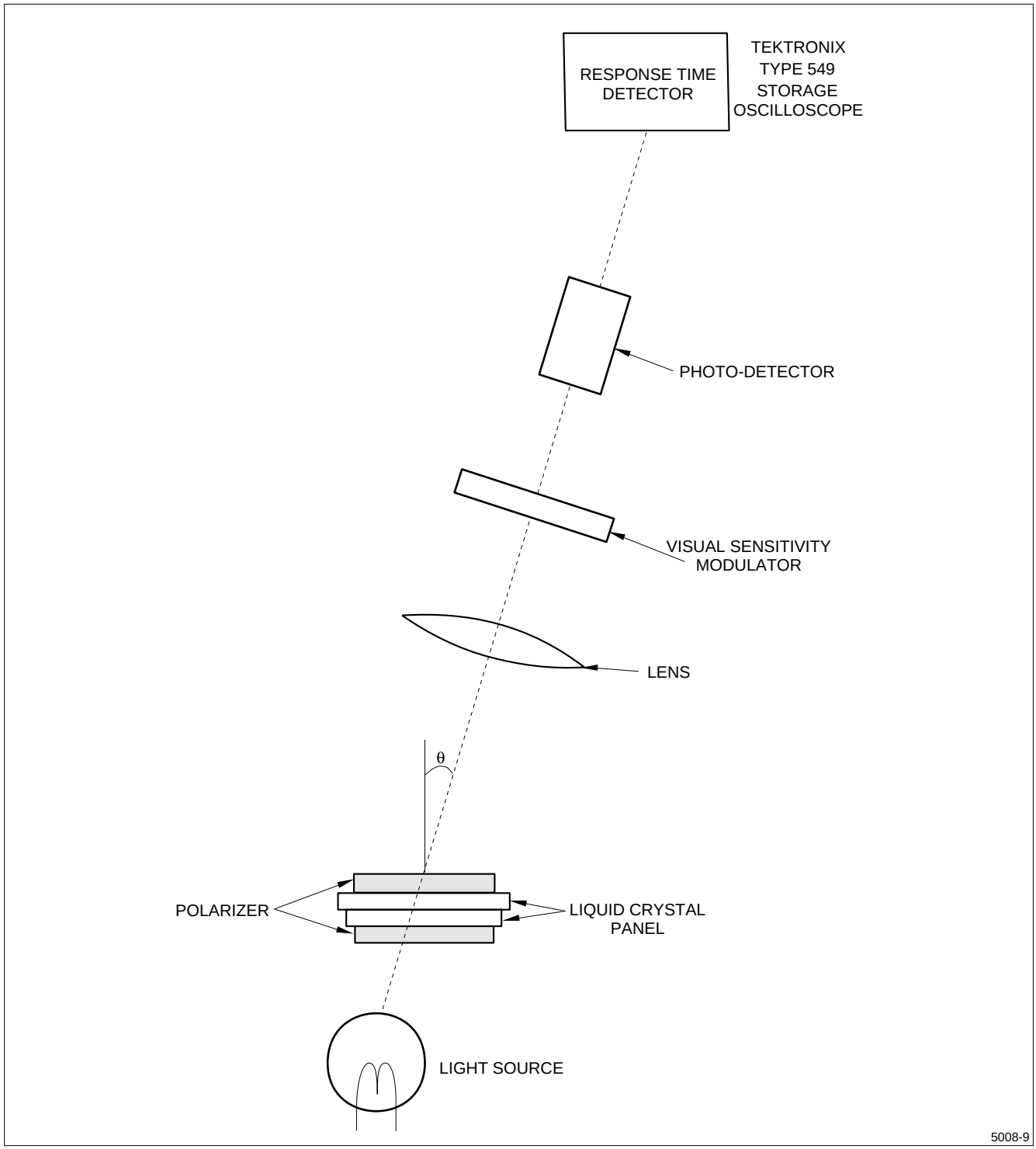



**Figure 9. Optical Characteristics Test Method II**

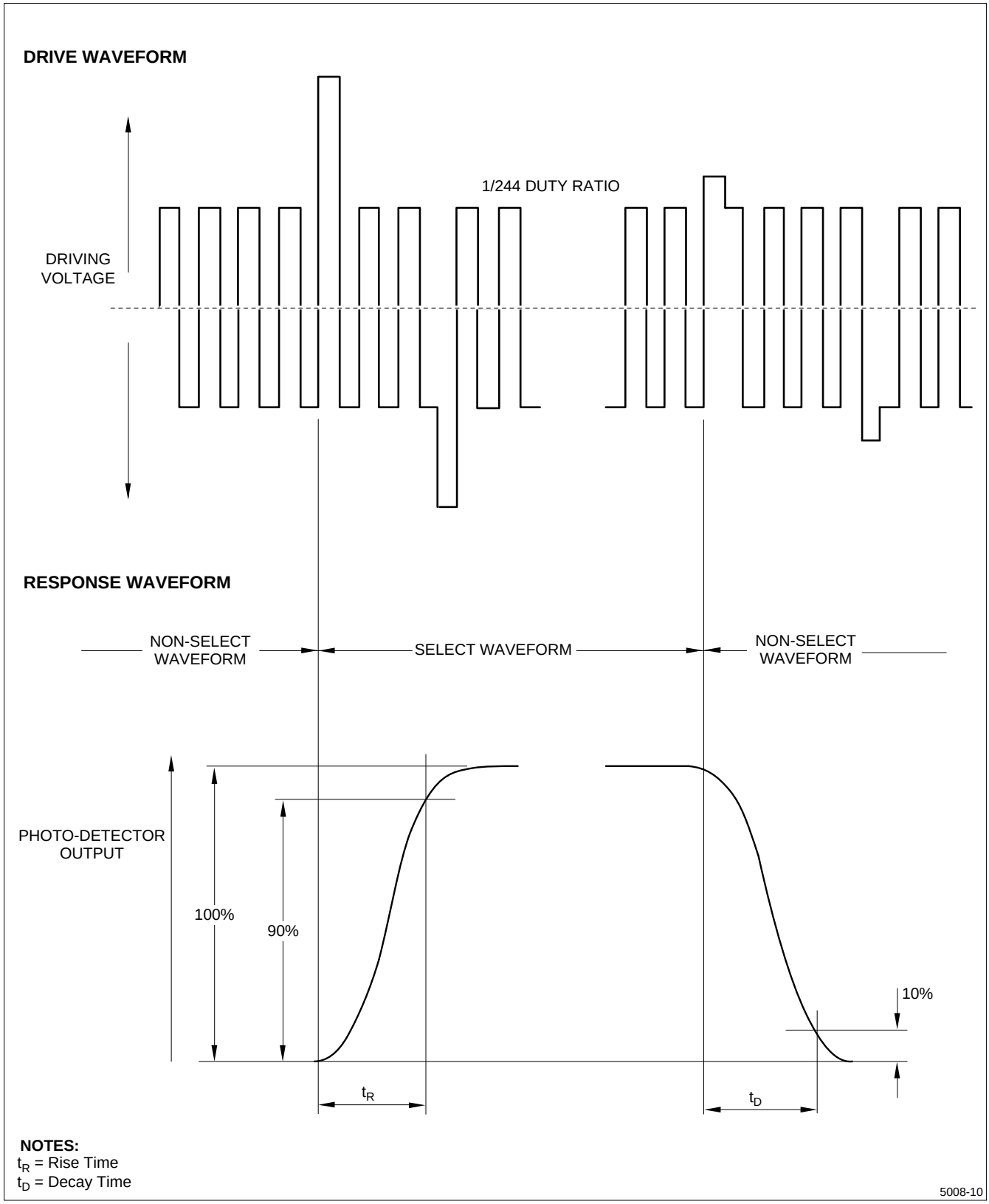



**Figure 10. Definition of Reponse Time**

## CHARACTERISTICS OF BACKLIGHT

The ratings are given on condition that the following conditions are satisfied.

### Rating

| PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|
| Brightness | 60 | 80 | – | $cd/m^2$ |

### Measurement Circuit

CXA-M10L (TDK) (at IL = 6 $mA_{RMS}$)

### Measurement Equipment

BM-7 (TOPCON)

### Measurement Conditions

- Measurement circuit voltage: DC = 11.0 V, at primary side.
- LCD: All digits WHITE, $V_{DD}$ = 5 V, $V_{EE} – V_{SS} = V_{MAX}$, $DU_0 – DU_7$ = 'H' (WHITE), $DL_0 – DL_7$ = 'H' (WHITE)
- Ambient temperature: 25°C. Make measurement 30 minutes after turning on the unit.

### Used Lamp Used (Ratings, 1pc.)[1]

FC2EX59/222T3/U3 Toshiba Lighting & Technology,. Ltd.)

| PARAMETER | | MAXIMUM ALLOWABLE VALUE | NOTE |
|---|---|---|---|
| Circuit Voltage (VS) | 1,200 $V_{RMS}$ (minimum) | – | 4 |
| Discharging Tube Current (IL) | 6 mA (typical) | 6.5 $mA_{RMS}$ | 2 |
| Power Consumption (P) | 2.5 W | – | 3 |
| Discharging Tube Voltage (VL) | 450 ±25 $V_{RMS}$ | 475 $V_{RMS}$ | – |
| Brightness (B) | 30,000 $cd/m^2$ (typical) | – | – |

**NOTES:**

1. Within no conductor closed (CCFT only).
2. It is recommended that IL be not more than 6 $mA_{RMS}$ so that heat radiation of CCFT backlight least affects the display quality.
3. Power consumption excluded inverter loss.
4. The circuit voltage (VS) of the inverter should be designed to have some margin (reference value: 1,500 $V_{RMS}$ minimum), since VS may be increased due to leak current in case of the LCD unit.

### Operating Life

The operating lifetime is 10,000 hours or more at 6 mA. (Operating life with CXA-M10L or equivalent).

The inverter should meet the following conditions:

- Sine, symmetric wave form without spike in positive and negative.
- Output frequency is from 25 kHz to 45 kHz.

Allow sufficient burn-in time before executing the operating conditions.

The operating lifetime is defined as having ended when any of the following conditions occur (25 ±1°C):

- When the voltage required for initial discharge has reached 1,320 $V_{RMS}$ or when it has reached 12.0 VDC when used as an inverter.
- When the illuminence or quantity of light has decreased to 60% of the initial value.

***NOTE:*** Ratings are defined as the average brightness inside the viewing area specified in Figure 11.

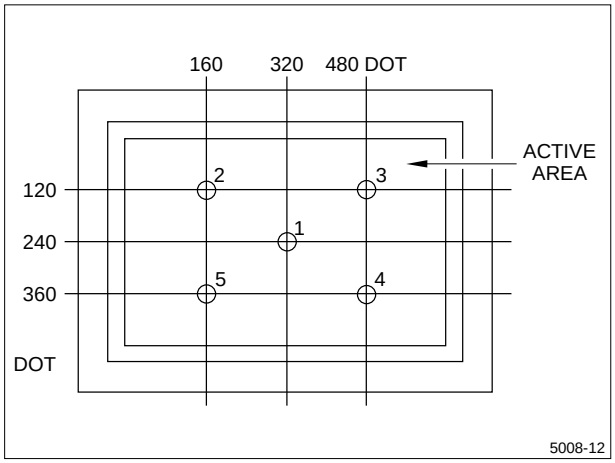



**Figure 11. Measuring Points (1 - 5)**

## PRECAUTIONS

- Industrial (Mechanical) design of the product in which this LCD unit is incorporated must be made so that the viewing angle characteristics of the LCD is optimized. This unit's viewing angle is illustrated in Figure 12 and as follows:
  - $\theta y$ MIN < viewing angle < $\theta y$ MAX
    (For the specific values of $\theta y$ MIN, $\theta y$ MAX, refer to the Optical Characteristics table. Consider the optimum viewing conditions according to the purpose when installing the unit.

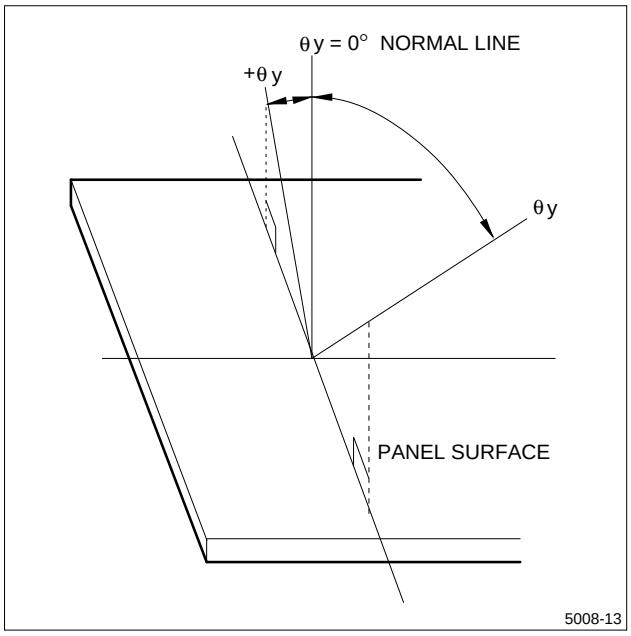



**Figure 12. Dot Matrix LCD Viewing Angle**

This unit is installed using mounting tabs at the four corners of PCB or bezel. During installation, avoid undue stress on the unit such as twisting or bending. A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.

- Since the front polarizer is easily damaged, use care to not scratch the face.
- If the surface of the LCD cells needs cleaning, wipe it with a soft cloth.
- Wipe liquid off immediately since it can cause color changes and staining.
- The LCD is made of glass plates. Use care when handling it to avoid breakage
- This unit contains CMOS LSIs which are sensitive to electrostatic charges. The following measures should be taken to protect the unit from electrostatic discharges:
  - Ground the metallic case of the main system (contact of the unit and main system).
  - Insulate the unit and main system by attaching insulating washers made of bakelite or nylon.
- The unit should be driven according to the specified ratings to avoid malfunction or permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating wave form by continuous application of the signal M. Avoid latch-up of driver LSIs and application of DC voltage to the LCD panel by following the ON/OFF sequence shown in Figure 13.
- Since leakage current, which may be caused by routing of CCFT cables, etc., may affect brightness of the display, the inverter has to be designed taking the leakage current into consideration. Thoroughly evaluate the LCD unit/inverter built into the host equipment to ensure the specified brightness.
- Do not expose the unit to direct sunlight, strong ultraviolet light, etc., for prolonged periods.
- Store the unit at normal room temperature to prevent the LC from converting to liquid (due to excessive temperature changes).
- Do not disassemble the unit.

***WARNING***: Don't use any materials which emit gas from epoxy resin (Amines' hardener) and silicone adhesive agent (dealcohol or deoxym) to prevent polarizer color owing to gas.

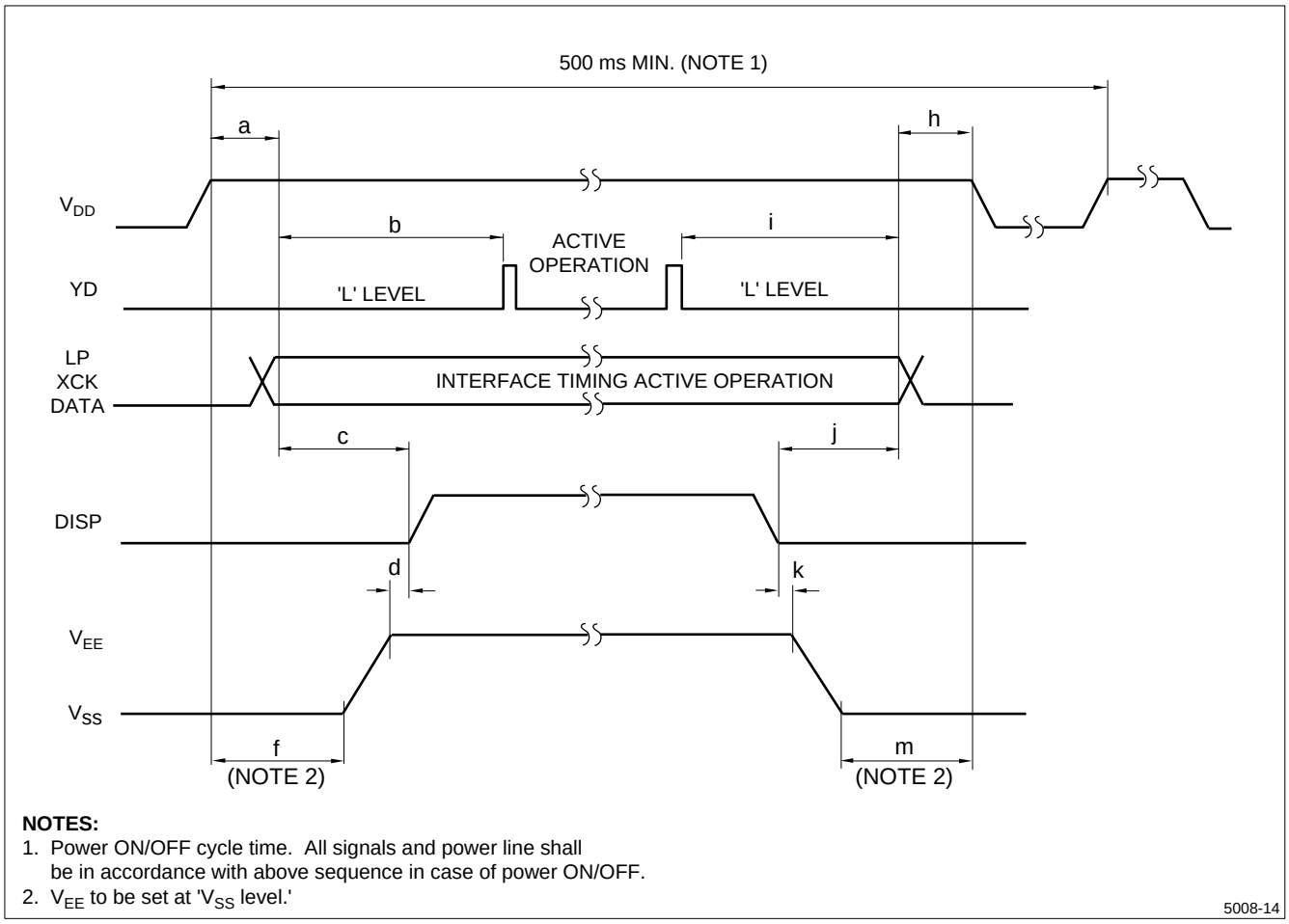



**Figure 13. Supply Voltage Sequence Condition**

| POWER ON | |
|---|---|
| **SYMBOL** | **CONDITION** |
| a | 0 ms (minimum) |
| b | 0 ms (minimum) |
| c | LP × 250 ms (minimum) |
| d | 0 ms (minimum) |
| f | 0 ms (minimum) |
| **POWER OFF** | |
| **SYMBOL** | **CONDITION** |
| h | 0 ms (minimum) |
| i | 0 ms (minimum) |
| j | 0 ms (minimum) |
| k | 0 ms (minimum) |
| m | 0 ms (minimum) |

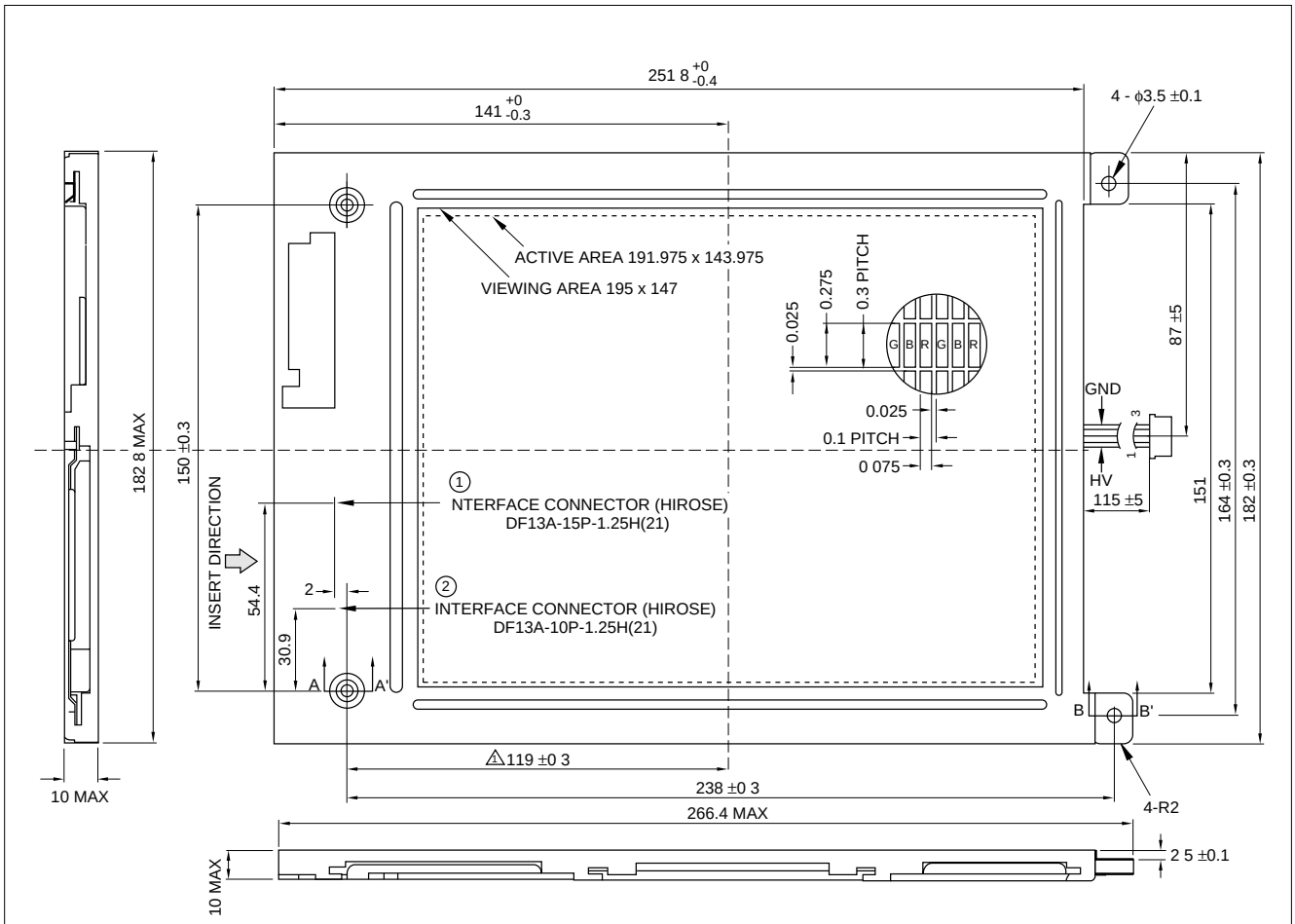
## APPLICABLE INSPECTION STANDARD

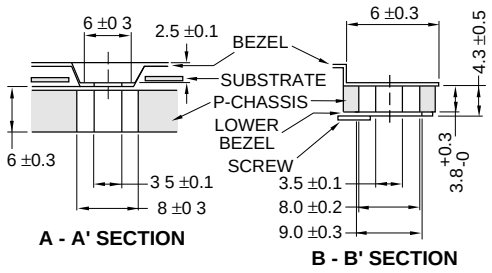
The LCD unit meets the following inspection standard: S-U-014

## DISPLAY QUALITY

This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, carefully evaluate display quality for the usability of the LCD unit in case gray scale is displayed on the LCD unit.

## OUTLINE DIMENSIONS

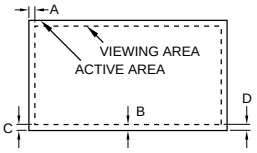



A - A' SECTION

B - B' SECTION

**BEZEL/DISPLAY POSITION**




① **INTERFACE CONNECTOR PIN LAYOUT**
DF13A-15P-1. 25H(21)
(HIROSE) (15 pins)

| PIN # | SIGNAL | PIN # | SIGNAL |
|---|---|---|---|
| 1 | YD | 9 | $DU_1$ |
| 2 | LP | 10 | $DU_2$ |
| 3 | XCK | 11 | $DU_3$ |
| 4 | DISP | 12 | $DU_4$ |
| 5 | $V_{DD}$ | 13 | $DU_5$ |
| 6 | $V_{SS}$ | 14 | $DU_6$ |
| 7 | $V_{EE}$ | 15 | $DU_7$ |
| 8 | $DU_0$ | | |

② **INTERFACE CONNECTOR PIN LAYOUT**
DF13A-10P-1.25H(21)
(HIROSE) (10 pins)

| PIN # | SIGNAL | PIN # | SIGNAL |
|---|---|---|---|
| 1 | $V_{SS}$ | 6 | $DL_4$ |
| 2 | $DL_0$ | 7 | $DL_5$ |
| 3 | $DL_1$ | 8 | $DL_6$ |
| 4 | $DL_2$ | 9 | $DL_7$ |
| 5 | $DL_3$ | 10 | $V_{SS}$ |

③ **CCFT CONNECTOR PIN LAYOUT**
CCFT Cable: UL3239. AWG22
CCFT Connector JST BHR-03VS-1

| PIN # | SIGNAL |
|---|---|
| 1 | HV |
| 2 | NC |
| 3 | GND |

**NOTES:**
1. Tolerance X-Direction A: 1.5 ±0.8
2. Tolerance Y-Direction B: 1.5 ±0.8
3. Obliquity of Display Area: IC-DI < 0 8
4. Signal Ground ($V_{SS}$) Connected with Metal Bezel
5. Unspecified Tolerance to be ±0.5

5008-15