

SKM 75GB124D



SEMITRANS™ 2

Low Loss IGBT Modules

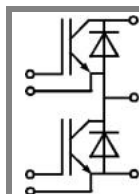
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Features

- MOS input (voltage controlled)
- N channel, homogeneous Si-structure (NPT-Non punch-through IGBT)
- Low loss high density chips
- Low tail current
- High short circuit capability, self limiting to $6 \times I_{Cnom}$
- Latch-up free
- Fast & soft inverse CAL diodes
- Isolated copper baseplate using DCB Direct Copper Bonding Technology without hard mould
- Large clearance (10 mm) and creepage distance (20 mm)

Typical Applications

- Switching (not for linear use)



GB

Absolute Maximum Ratings		$T_c = 25\text{ }^\circ\text{C}$, unless otherwise specified	
Symbol	Conditions	Values	Units
IGBT			
V_{CES}	$T_c = 25\text{ (75) }^\circ\text{C}$	1200	V
I_C	$t_p = 1\text{ ms}$	100 (75)	A
I_{CRM}		100	A
V_{GES}		± 20	V
T_{vj} (T_{stg})	$T_{OPERATION} \leq T_{stg}$	- 40 ... + 150 (125)	$^\circ\text{C}$
V_{isol}	AC, 1 min.	2500	V
Inverse diode			
I_F	$T_c = 25\text{ (80) }^\circ\text{C}$	75 (50)	A
I_{FRM}	$t_p = 1\text{ ms}$	100	A
I_{FSM}	$t_p = 10\text{ ms}$; sin.; $T_j = 150\text{ }^\circ\text{C}$	550	A

Characteristics		$T_c = 25\text{ }^\circ\text{C}$, unless otherwise specified			
Symbol	Conditions	min.	typ.	max.	Units
IGBT					
$V_{GE(th)}$	$V_{GE} = V_{CE}$, $I_C = 2\text{ mA}$	4,5	5,5	6,5	V
I_{CES}	$V_{GE} = 0$, $V_{CE} = V_{CES}$, $T_j = 25\text{ (125) }^\circ\text{C}$		0,1	0,3	mA
$V_{CE(TO)}$	$T_j = 25\text{ (125) }^\circ\text{C}$		1,1 (1,1)	1,25 (1,25)	V
r_{CE}	$V_{GE} = 15\text{ V}$, $T_j = 25\text{ (125) }^\circ\text{C}$		20 (2,6)	2,4 (3,2)	m Ω
$V_{CE(sat)}$	$I_{Cnom} = 50\text{ A}$, $V_{GE} = 15\text{ V}$, chip level		2,1 (2,4)	2,45 (2,85)	V
C_{ies}	under following conditions		3,3	4,3	nF
C_{oes}	$V_{GE} = 0$, $V_{CE} = 25\text{ V}$, $f = 1\text{ MHz}$		0,5	0,6	nF
C_{res}			0,22	0,3	nF
L_{CE}				30	nH
$R_{CC'+EE'}$	res., terminal-chip $T_c = 25\text{ (125) }^\circ\text{C}$		0,75 (1)		m Ω
$t_{d(on)}$	$V_{CC} = 600\text{ V}$, $I_{Cnom} = 50\text{ A}$		60	100	ns
t_r	$R_{Gon} = R_{Goff} = 22\text{ }\Omega$, $T_j = 125\text{ }^\circ\text{C}$		55	100	ns
$t_{d(off)}$	$V_{GE} = \pm 15\text{ V}$		420	500	ns
t_f			50	100	ns
E_{on} (E_{off})			8 (6)		mJ
Inverse diode					
$V_F = V_{EC}$	$I_{Fnom} = 50\text{ A}$; $V_{GE} = 0\text{ V}$; $T_j = 25\text{ (125) }^\circ\text{C}$		2 (1,8)	2,5	V
$V_{(TO)}$	$T_j = 25\text{ (125) }^\circ\text{C}$		1,1	1,2	V
r_T	$T_j = 25\text{ (125) }^\circ\text{C}$			22	m Ω
I_{RRM}	$I_{Fnom} = 50\text{ A}$; $T_j = 125\text{ () }^\circ\text{C}$		39		A
Q_{rr}	$di/dt = \text{A}/\mu\text{s}$		7		μC
E_{rr}	$V_{GE} = V$				mJ
Thermal characteristics					
$R_{th(j-c)}$	per IGBT			0,27	K/W
$R_{th(j-c)D}$	per Inverse Diode			0,6	K/W
$R_{th(c-s)}$	per module			0,05	K/W
Mechanical data					
M_s	to heatsink M6	3		5	Nm
M_t	to terminals M5	2,5		5	Nm
w				160	g

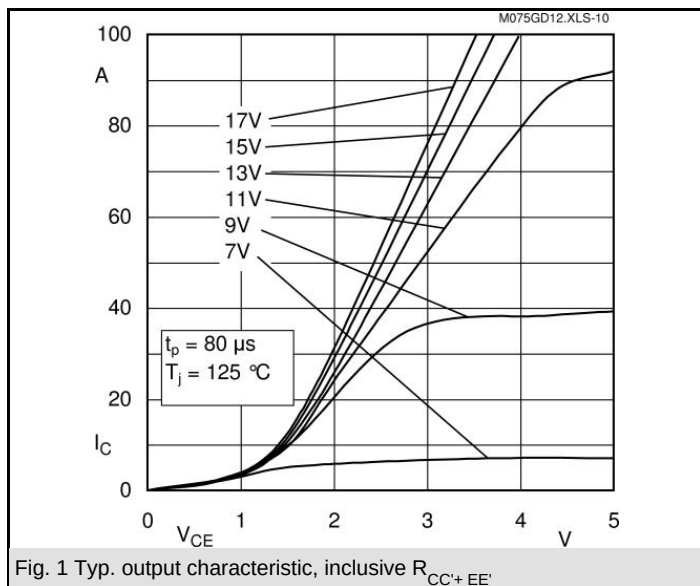


Fig. 1 Typ. output characteristic, inclusive $R_{CC'+EE'}$

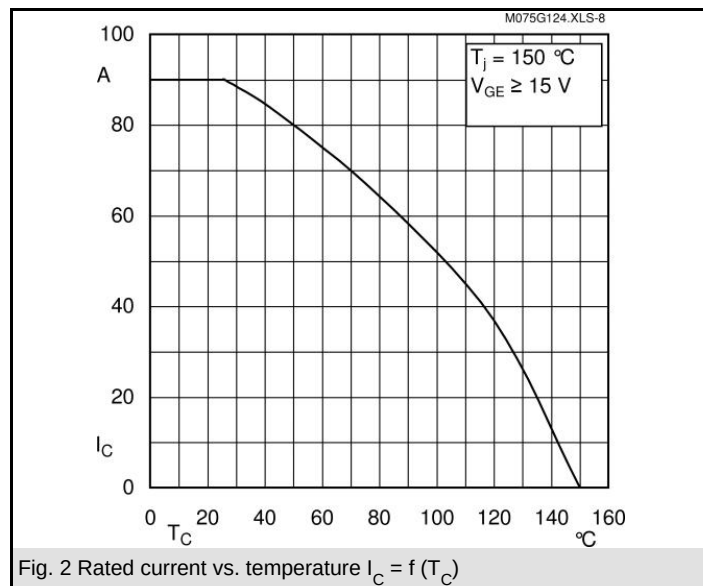


Fig. 2 Rated current vs. temperature $I_C = f(T_C)$

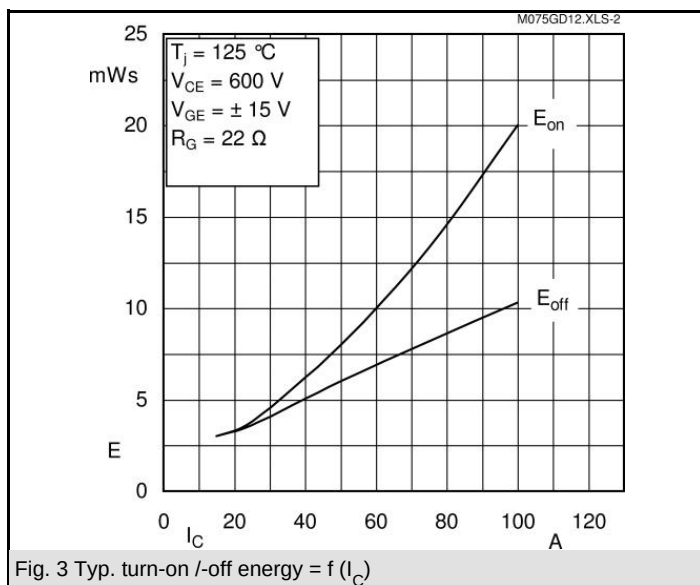


Fig. 3 Typ. turn-on /off energy = $f(I_C)$

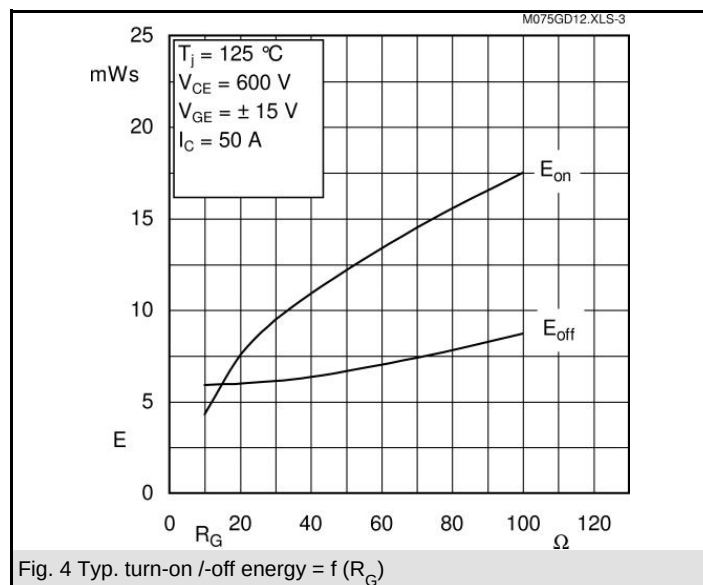


Fig. 4 Typ. turn-on /off energy = $f(R_G)$

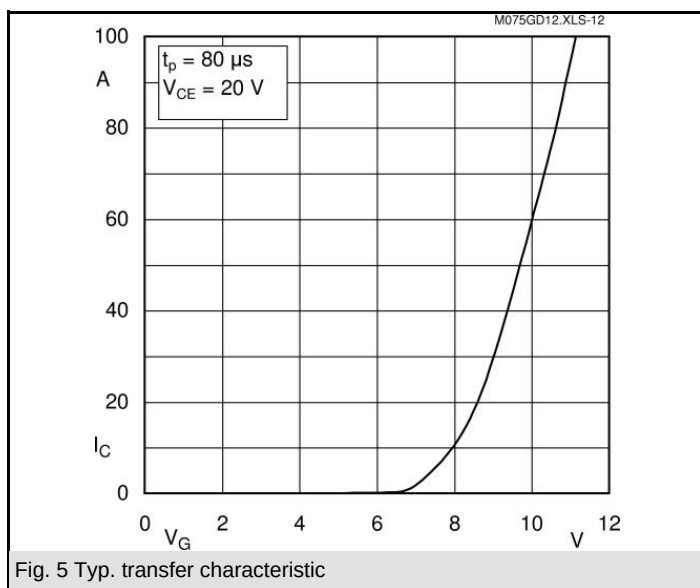


Fig. 5 Typ. transfer characteristic

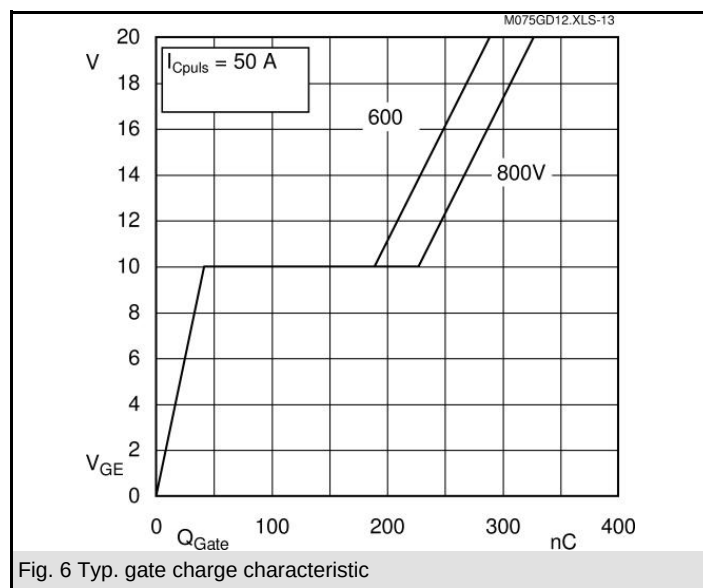
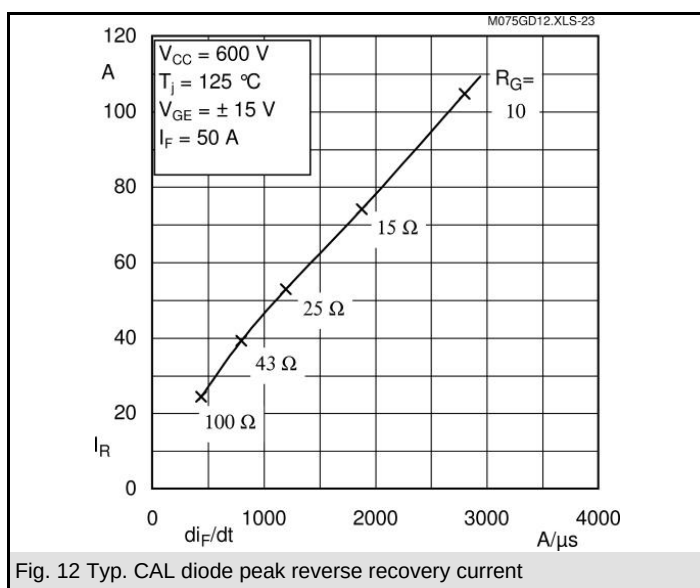
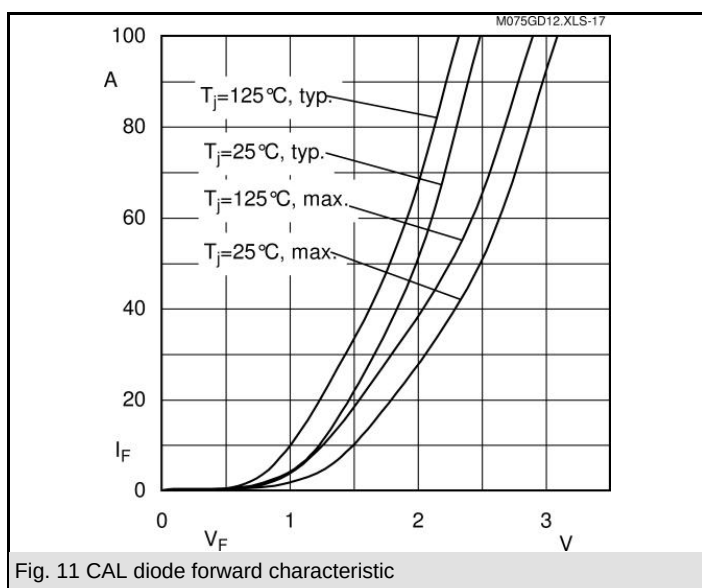
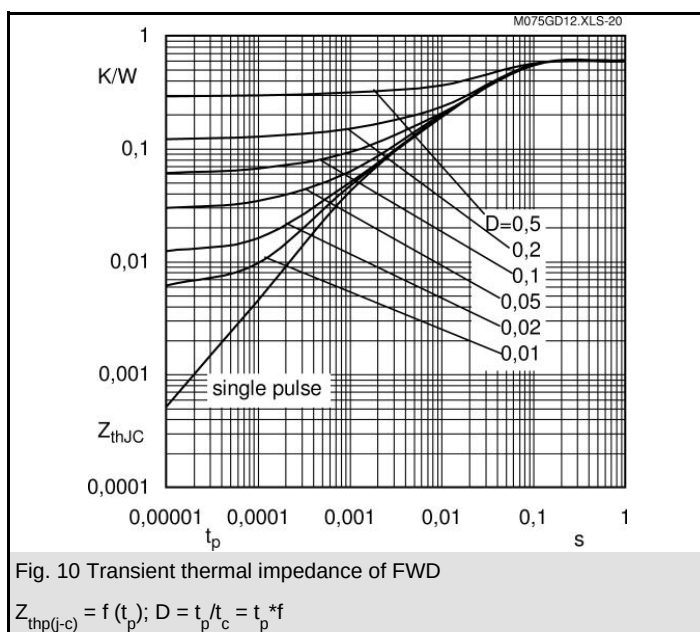
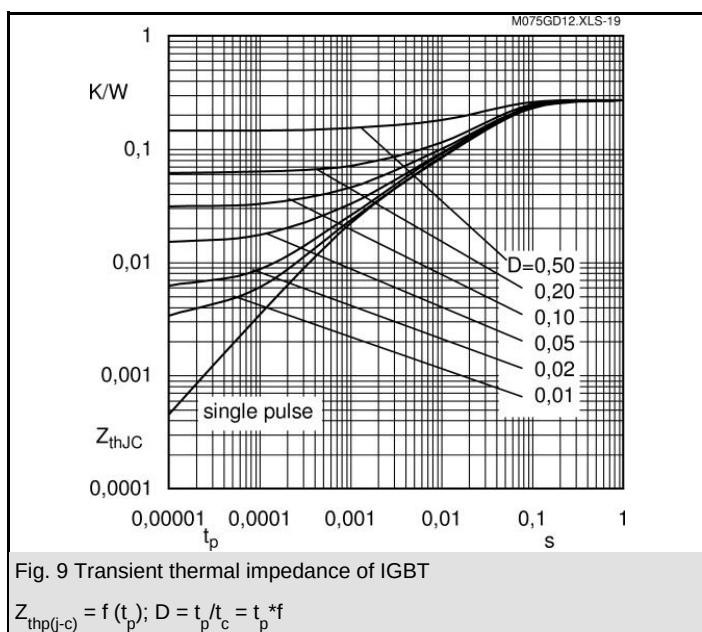
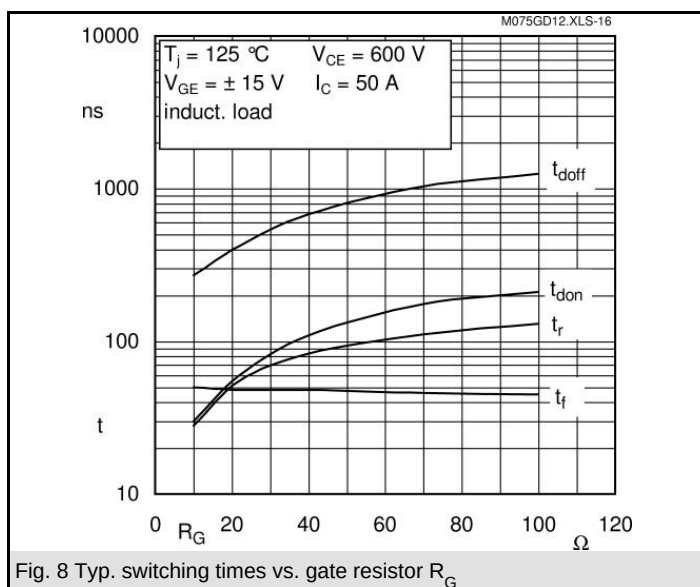
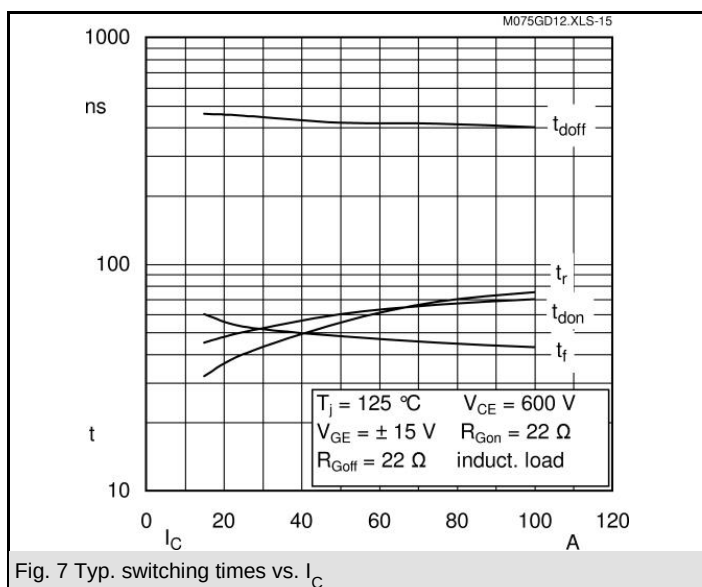
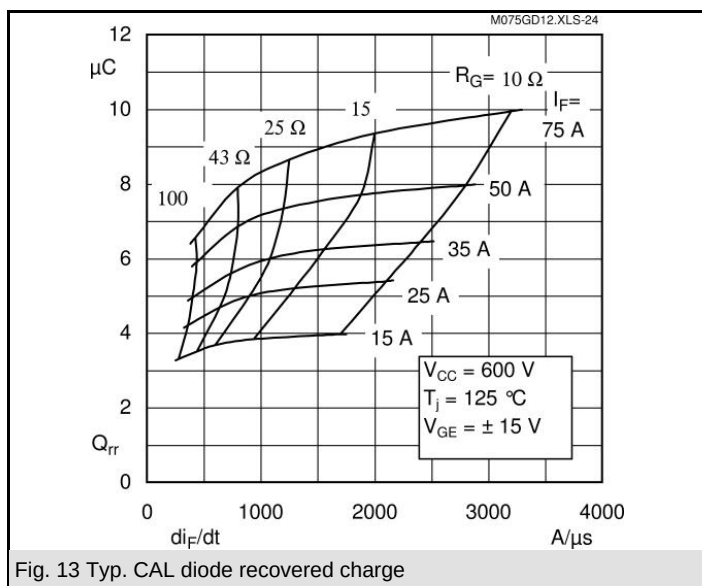


Fig. 6 Typ. gate charge characteristic



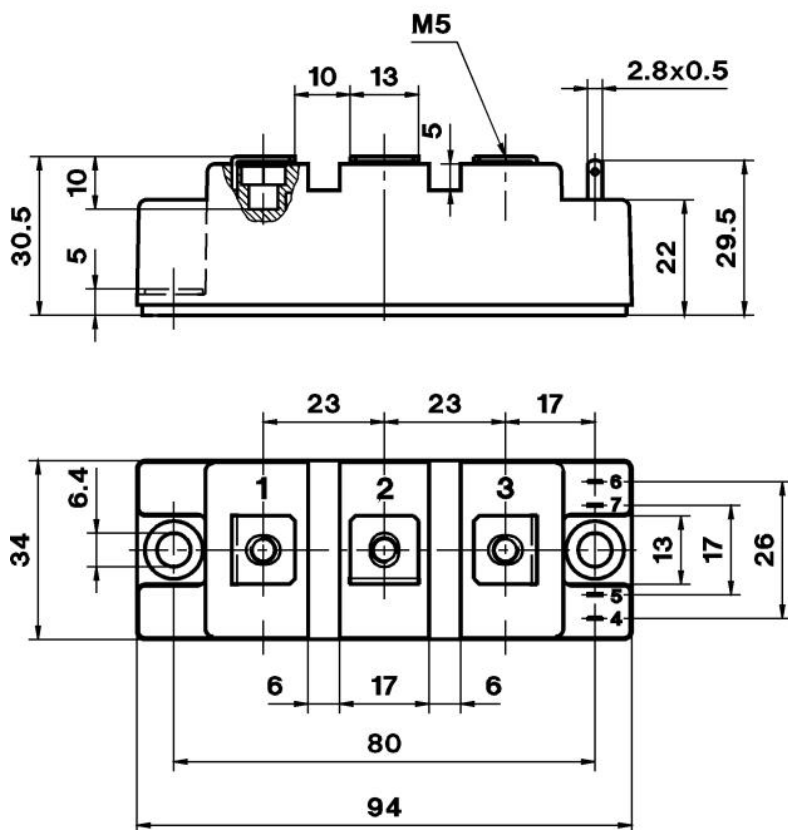
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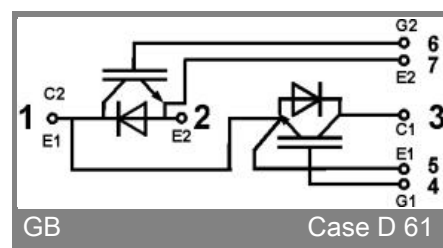
UL Recognized
File no. E 63 532

Dimensions in mm

CASED61



Case D 61



This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX.

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